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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/686,486
Filing Date: October 15, 2003
Appellant(s): CHEUNG ET AL.

Keith Tackett
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed 22 January 2007 appealing from the Office action mailed 26 May 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is substantially correct. The changes are as follows:

WITHDRAWN REJECTIONS

The following grounds of rejection are not presented for review on appeal because they have been withdrawn by the examiner. All rejections under 35 USC 102(e) based on any of the Dordi et al references have been withdrawn in view of the petition under 37 CFR 1.78 to add a priority claim to application no. 09/263,126, which petition was granted on 15 May 2007.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

US 5,297,910	Yoshioka et al	3-1994
US 5,980,706	Bleck et al	11-1999
US 6,123,825	Uzoh et al	9-2000
US 6,155,275	Shinbara	12-2000

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

---Claim 15 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al (US 5,297,910) in view of Bleck et al (US 5,980,706) and Uzoh et al (US 6,123,825).

Yoshioka et al teach (see figure 1) a system for treatment of semiconductor wafers including a mainframe (12) having a transfer robot (14) therein, a loading station (30) disposed in connection with the mainframe (12), wherein the loading station included a transfer robot (38) and multiple processing stations (20-24) in connection with the mainframe.

However, Yoshioka et al do not teach that the processing stations included one or more electrochemical deposition cells and one or more post deposition treatment chambers.

Bleck et al teach (see abstract and figure 1) processing stations for semiconductor wafers wherein an electrochemical deposition treatment was carried out.

Therefore, it would have been obvious to one of ordinary skill in the art to have incorporated the electrochemical deposition chambers of Bleck et al into the mainframe wafer processing system of Yoshioka et al in order to allow more complete processing of the wafers within the single system.

Uzoh et al teach (see cols. 7-8) that after formation of an electroplated copper layer on semiconductor wafers, it was customary to perform annealing of the copper layer to ensure small grain size of the copper within the layer.

Therefore, it would have been obvious to one of ordinary skill in the art to have added a conventional post deposition treatment annealing chamber to the system of Yoshioka et al and Bleck et al in order to perform the conventional annealing step to ensure proper grain size of the electroplated copper layer.

---Claim 20 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yoshioka et al (US 5,297,910) in view of Bleck et al (US 5,980,706) and Shinbara (US 6,155,275) and further in view of Uzoh et al (US 6,123,825).

Yoshioka et al teach (see figure 1) a system for treatment of semiconductor wafers including a mainframe (12) having a transfer robot (14) therein, a loading station (30) disposed in connection with the mainframe (12), wherein the loading station included a transfer robot (38) and multiple processing stations (20-24) in connection with the mainframe. The system of Yoshioka et al included multiple identical processing stations to allow an increased throughput by parallel processing of wafers at the different stations.

However, Yoshioka et al do not teach that the processing stations included one or more electrochemical deposition cells and one or more post deposition treatment chambers.

Bleck et al teach (see abstract and figure 1) processing stations for semiconductor wafers wherein an electrochemical deposition treatment was carried out.

Therefore, it would have been obvious to one of ordinary skill in the art to have incorporated the electrochemical deposition chambers of Bleck et al into the mainframe wafer processing system of Yoshioka et al in order to allow more complete processing of the wafers within the single system.

Shinbara teaches (see figure 1 and related description) a wafer processing apparatus including a spin-rinse-dry station (U3) for cleaning the wafers after processing.

Therefore, it would have been obvious to one of ordinary skill in the art to have included a spin-rinse-dry station as taught by Shinbara in the apparatus of Yoshioka et al and Bleck et al for the purpose of cleaning the wafers after the electrodeposition process.

Shinbara does not teach that the loading station robot transferred wafers from the cassettes to the spin-rinse-dry modules. However, it would have been obvious to one of ordinary skill in the art to have placed the stations at any convenient location with respect to the loading station robot without otherwise affecting the operation of the apparatus. See MPEP 2144.04.VI.C. A motivation to perform this rearrangement would be to allow easy access for preliminary rinsing/cleaning and for final

rinsing/cleaning of processed wafers, such that the first and last station the wafers are treated at are the spin-rinse-dry stations.

Uzoh et al teach (see cols. 7-8) that after formation of an electroplated copper layer on semiconductor wafers, it was customary to perform annealing of the copper layer to ensure small grain size of the copper within the layer.

Therefore, it would have been obvious to one of ordinary skill in the art to have added a conventional post deposition treatment annealing chamber to the system of Yoshioka et al and Bleck et al in order to perform the conventional annealing step to ensure proper grain size of the electroplated copper layer.

(10) Response to Argument

Appellant has argued:

(a) Uzoh et al teach a process involving an annealing step, not the structure of an annealing chamber.

In response, Appellants attention is directed to paragraph [0093] of the specification as filed. In that paragraph, Applicant admitted that "[t]hermal anneal process chambers are generally well known in the art". Thus, the Examiner finds that given the teachings of Uzoh et al, one of ordinary skill in the art would have been motivated to have added one of these generally well known (i.e.-conventional) thermal anneal chambers to the mainframe of Yoshioka et al in view of Bleck et al.

(b) Uzoh et al do not suggest placing an annealing chamber in connection with a mainframe.

In response, given the level of skill of one of ordinary skill in the art and the teachings of Yoshioka et al, it would have been obvious to have incorporated all needed processing stations into the mainframe. In particular, the automated mainframe system obviates the need for user handling of individual wafers, such that by incorporating multiple, sequential treatment stations within a single housing, multiple processing steps can occur without the need for human intervention. Thus, with this desire in mind, it would have been obvious to one of ordinary skill in the art to have incorporated a conventional thermal annealing chamber in connection with the mainframe of Yoshioka et al in view of Bleck et al.

(c) The combination of Yoshioka et al, Bleck et al, Uzoh et al and Shinbara do not teach one or more rapid thermal anneal chambers in connection with the loading station.

In response, claim 20 does not recite "rapid thermal anneal chambers", merely "thermal anneal chambers". Further, Appellant has failed to show that the claim term "in connection with a loading station" means anything more than "associated with". Placing a chamber within the mainframe is deemed to meet this claim term, as the entire mainframe is considered to be "in connection with the loading station". Applicant is relying on specific embodiments from the specification (e.g.-figure 3), where the thermal anneal chambers (211) were arranged adjacent to the loading station (210), but not adjacent to the mainframe (218). However, the claims are given their broadest reasonable interpretation, and the claims terms do not limit the post deposition treatment chambers to be adjacent to the loading station and not the mainframe.

(d) The combination of Yoshioka et al, Bleck et al, Uzoh et al and Shinbara do not teach two or more spin-rinse-dry modules in connection with the loading station.

In response, Yoshioka et al teach (see col. 9, lines 22-27) that increased throughput can be achieved by including multiple treatment stations to permit parallel treatment of wafers. Therefore, it would have been obvious to one of ordinary skill in the art to have included multiple chambers/modules for the purpose of increasing the throughput of the system. The Examiner's remarks with respect to point (c) are incorporated herein to address Appellant's remarks regarding the spin-rinse-dry module being "in connection with the loading station". Further, since the post-deposition treatment stations were the location of the final treatments of the wafers, it would have been obvious to have placed those stations at a location near the loading station so that the wafers could be easily returned to the cassettes (42, 44).

Based on Appellants' remarks and additional claim interpretation by the Examiner, if the term "in connection with the loading station" in claim 20 were to be interpreted in the manner that Appellant has argued, i.e.-"adjacent to", claim 15 would be considered unsupported by the specification as filed, since it requires the "post deposition treatment chambers [thermal anneal chambers] disposed in connection with the mainframe". It is clear from Appellants' drawings that the thermal anneal chambers (211) were not adjacent to the mainframe (218), but were adjacent to the loading station (210). Thus, the language utilized by Appellant should be construed consistently across all of the claims, such that "in connection with" is not interpreted to mean "adjacent to", but merely means that the two are part of the same system.

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

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